a thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall filled with a plating layer having a surface to form a viahole having a diameter , wherein:

the surface of said plating layer extending out of the through-holes and lying in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies; and

the thickness of said conductor circuit layer being less than a half of the viahole diameter.

Cont'd B1

2. The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall of the through-hole is roughened.

3. The multilayer printed wiring board as set forth in Claim 1, wherein the plating layer surface and conductor circuit layer extending out of the through-holes are roughened.

4. The multilayer printed wiring board as set forth in Claim 1, wherein at least one of the surfaces of the conductor circuits are roughened.

5. The multilayer printed wiring board as set forth in Claim 1, wherein a further viahole is formed in the viahole.

B2 7. The multilayer printed wiring board as set forth in Claim 1, wherein a ratio

between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

8. The multilayer printed wiring board as set forth in Claim 1, wherein the conductor circuit layer has a thickness less than 25 μm.

9. A multilayer printed wiring board comprising conductor circuit layers having a thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall filled with a plating layer having at least one surface to form a viahole having a diameter, wherein the thickness of said conductor circuit layer is less than a half of the viahole diameter and less than 25 μm.

10. The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall of the through-holes is roughened.

11. The multilayer printed wiring board as set forth in Claim 9, wherein a depression is formed on a central surface portion of the plating layer surface extending out of the through-holes.

12. The multilayer printed wiring board as set forth in Claim 9, wherein the surface of the plating layer and the surface of the conductor circuit layer extending out of the through-holes are roughened.

13. The multilayer printed wiring board as set forth in Claim 9, wherein at least

cont'd B2

one of the surfaces of the conductor circuit layer is roughened.

14. The multilayer printed wiring board as set forth in Claim 9, wherein a further viahole is formed in the viahole.

16. The multilayer printed wiring board as set forth in Claim 9, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

17. A multilayer printed wiring board comprising conductor circuit layers each with at least one surface wherein at least one of the surfaces of the conductor circuit layer

B3

is roughened and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall wherein the inner wall is roughened, filled with a plating layer to form a viahole, wherein:

said roughened inner wall is covered with a roughened electroless plating layer; and

an inner space of said through-hole defined by the electroless plating layer and is filled with an electroplating layer.

18. The multilayer printed wiring board as set forth in Claim 17, wherein depressions are formed in the central surface portion of the plating layer surface extending out of the through-holes.

19. The multilayer printed wiring board as set forth in Claim 17, wherein the plating layer surface and conductor circuit surface extending out of the through-holes are

roughened.

21. The multilayer printed wiring board as set forth in Claim 17, wherein a further viahole is formed in the viahole.

23. The multilayer printed wiring board as set forth in Claim 17, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

24. The multilayer printed wiring board as set forth in Claim 17, wherein the conductor circuit layer has a thickness less than 25 μm.

25. A multilayer printed wiring board comprising conductor circuit layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall, filled with a plating layer to form a viahole,

said interlaminar insulative resin layers being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

26. The multilayer printed wiring board as set forth in Claim 25, wherein the interlaminar insulative resin layer is made of a composite of fluororesin fiber cloth, wherein said cloth comprises voids, and wherein thermosetting resin is impregnated in the voids in

the cloth.

27. The multilayer printed wiring board as set forth in Claim 25, wherein the inner wall of the through-holes is roughened.

28. The multilayer printed wiring board as set forth in Claim 25, wherein depressions are formed in the central surface portion of the plating layer surface extending out of the through-holes.

29. The multilayer printed wiring board as set forth in Claim 25, wherein the plating layer surface and conductor circuit surface extending out of the through-holes are roughened.

31. The multilayer printed wiring board as set forth in Claim 25, wherein a further viahole is formed in the viahole.

32. The multilayer printed wiring board as set forth in Claim 25, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

33. The multilayer printed wiring board as set forth in Claim 25, wherein the conductor circuit layer has a thickness less than 25 μm.

REMARKS

Reconsideration and withdrawal of the rejections in the Office Action are